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Design Freedom in Multilayer Thin-Film Devices

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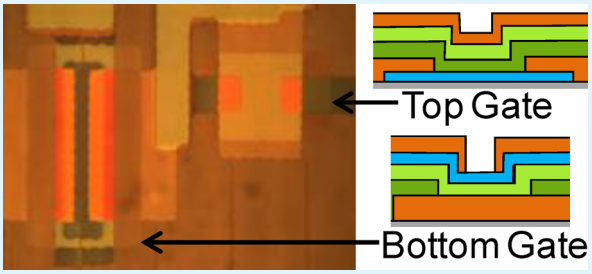
Supporting Information

ABSTRACT: In fabricating inorganic thin-film devices, the relative etch rates of materials in a given etch chemistry often limit the obtainable multilayer structures. Alternatively, in fabricating multilayer organic devices by solution processing, the ability to formulate the active organic materials in orthogonal solvent systems is limiting. The pattered-by-printing method uses the combination of selective area deposition (SAD) and atomic layer deposition (ALD) to form high-quality metal oxide thin-film devices. We print an inhibiting polymer ink that patterns the functional inorganic materials that are deposited via spatial ALD (SALD). The process is inherently orthogonal, as the polymer ink does not etch or swell the inorganic functional layers. Each functional layer is additively patterned as deposited, with device isolation and vias defined by the printed inhibitor. The combination of process orthogonality and additive patterning removes processing-related constraints on device design, and readily allows for any combination of bottom- and top-gate thin-film transistor architectures to be formed on the same substrate. The freedom of this approach is further demonstrated by both all-enhancement-mode circuits and enhancement-depletion-mode circuits. In addition, we present a new tool to tune circuit performance by local control of dielectric thickness.



KEYWORDS: *additive process, thin-film, printed electronics, ALD, selective area deposition, ZnO, circuit design*

INTRODUCTION

We have been investigating the use of selective area deposition (SAD) in combination with atomic layer deposition (ALD), making devices that are "patterned-by-printing".[1−5] Our model patterned-by-printing system uses inkjet-printed polyvinylpyrrolidone (PVP) to selectively deposit ZnO, Al_2O_3 and aluminum doped-ZnO (AZO) by SALD to form thin-film devices. Although we use these techniques for fabricating thin-film electronics, patterned-by-printing is useful for fabricating any thin-film inorganic device whose layers can be deposited by ALD, such as optical or magnetic devices. Additionally, the design freedom that comes from the orthogonal nature of the processing is extendable to other selective area deposition systems (beyond ALD).

Materials deposition is done using SALD, with the distinguishing term "spatial" being indicative of a spatially sequential exposure to precursors rather than the temporally sequential exposure used in the more traditional chamber-based ALD.[6−10] In chamber-based ALD, cycle times are typically long, due to the time that it takes to remove (purge) each precursor gas from the vacuum chamber, often on the order of seconds.[11,12] In contrast, the precursors and purge gases flow at steady state through a SALD deposition head, and the substrate surface receives sequential precursor exposure by moving the substrate relative to the deposition head.[7] Because the SALD gas-exposure time is controlled by the relative velocity of the SALD head and the substrate, SALD cycle times are generally limited by kinetics (the time for the chemical reaction of the precursors with the substrate) rather than by any limitation of the equipment.[9] This allows for very short cycle times, 200 ms or less, which we have shown are advantaged for SAD patterning of ALD thin-films.[4] In our SALD system, the deposition takes place at atmospheric pressure without an enclosure, which provides an additional process advantage by removing the need to pump-down a reaction chamber.[7]

SAD, the other key technology that enables the patterned-by-printing approach, refers to a process in which a portion of a substrate surface is modified to prevent, or inhibit, material deposition. Many groups have explored different materials that influence ALD growth on a surface, with inhibitor materials typically selected from self-assembled monolayers (SAMs) of silanes,[13−15] or polymers.[16−18] The patterned-by-printing technique uses polymer inhibitor materials, and is practiced under conditions where there is substantially no growth on the inhibitor surface. This regime is more reliable than, and is distinct from, a lift-off regime sometimes used in SAD systems with metal oxides.[17] In practice, it is far easier to pattern and remove polymer inhibitors than the more studied SAMs, and polyvinylpyrrolidone (PVP), which is easily formulated into ink for printing, is our primary printed inhibitor.[1−5] Although the benefits of SAD patterning are independent of the method used to deposit the inhibitor, by using digital printing, we can rapidly screen variations on a design theme, allowing for circuits to go from desktop design to electrical operation in less than 1 day.[19]

This combination of the SALD and SAD technologies brings advantages in both throughput and process speed.[4] These

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advantages do not come at a cost penalty for performance, as we have previously reported, thin-film transistors (TFTs) fabricated using the patterned-by-printing approach have equivalent performance as TFTs of the same materials fabricated using traditional photolithographic techniques.[2,3] These high performance TFTs make patterned-by-printing electronics a potential manufacturing technology for multiple applications. For example, ALD-deposited ZnO-based thin-film electronics could compete with the sputtered GIZO that is becoming the work-horse material for OLED backplanes. For high-speed electronics, SAD is being investigated to pattern the high-k dielectric materials that are currently deposited by ALD, because of the difficulty of using etching to pattern these materials.[20] As noted, SALD is our preferred ALD system, with its potential for use in roll-to-roll manufacturing of flexible electronics and photovoltaics.[7] Overall, the combination of the as-deposited material performance of semiconductors, transparent conductors and dielectrics, the printed nature of the patterning, and the large-area compatibility of the process, makes patterned-by-printing attractive for the high-speed production of printed electronics.

Here, we will first illustrate how the patterned-by-printing process works for generalized multilayered structures, without specific attention to electronics. The key to the design freedoms is the ability to independently control the vertical position of interfaces and the in-plane pattern of the materials. This three-dimensional patterning process allows for within-device variations, and device-to-device variations on a single substrate. Using those fundamentals, we expand beyond the bottom-gate transistor architecture that we have used in the past. Continuing to build upon the freedoms allowed by patterned-by-printing, we integrate individual TFTs into both enhancement-mode and enhancement-depletion mode circuits.

PATTERNING FREEDOM

To illustrate the scope of the technique, we examine patterned-by-printing as applied to three sequentially deposited patterned layers of material, as shown in Figure 1. (See Figure S1 for plan views of the three patterns and corresponding plan view of the cross-section shown in Figure 1.) Using selective deposition to pattern each layer allows for eight possible layer combinations to be independently patterned on the substrate, using three inhibitor patterns paired with three SALD depositions. The eight combinations of layers A, B and C are (1) just layer A; (2) just B; (3) just C; (4) layers A and B; (5) layers A and C; (6) layers B and C; (7) all layers, A, B and C; (8) no layers at all, as shown in Figure 1.

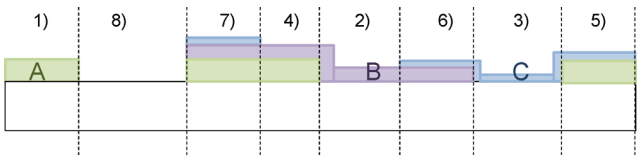

Figure 1. Eight possible layer combinations from three sequentially deposited patterned layers. Each of the eight layer stacks as shown is equally easy to achieve, and is a consequence of the pattern of inhibitor used to pattern each layer A, B, or C. Plan views of the three inhibitor patterns and the final growth pattern can be found in Figure S1 of the Supporting Information.

The process steps consist of applying a patterned inhibitor, depositing the material via ALD, and cleaning the substrate. As shown, layer A could be 100 nm of AZO, layer B 50 nm of Al_2O_3, and layer C 20 nm of ZnO, each layer having a unique thickness and composition. Alternatively, the thickness of a single material can be varied in a patterned manner by building up multiple thin layers of that material. This approach is particularly useful in forming variable thickness dielectric layers on a substrate, for example, in order to provide extra prevention against shorting between conductive lines ("crossover dielectric") without increasing the gate dielectric thickness.

The combination of SALD and SAD has no preferred layer order, either for materials or for patterns. Devices containing many layers can be built alongside devices with far fewer layers. Devices can share any number of layers in common. This independence of patterning and material properties translates directly into design advantages when building thin-film electronics. For example, a via (i.e., a hole) in a layer of a material using this approach, is created by printing a pattern of inhibitor in the size and shape of the required via.

In addition to the patterning possibilities described in relationship to Figure 1, a single inhibitor printing step can be used to pattern multiple materials layers. Our analysis of inhibitor failure has shown that the inhibitor is effective until there is nucleation of growth on the inhibitor surface.[4] When the combined desired inorganic thin-film thickness remains below the inhibition failure thickness, it is possible to pattern two or more layers of material using the same inhibitor pattern. This ability to print once, and to pattern the growth of multiple SALD layers, enables control of interfaces between layers of different materials.[19] This feature also enables the creation of aligned patterns of different materials without the error associated with alignment of another patterning step.

Each material has a maximum inhibition thickness for a given set of process conditions.[4] This limitation can be overcome in practice, however, by using a multilayer stack, as there is no limit to the number of layers that can be formed on top of each other using successive print-SALD-clean cycles. This means that, for example, although the limit on the inhibition thickness of an inkjet-printed layer of PVP for DMAI-grown alumina is ~60 nm at our usual conditions, devices can be built with far more dielectric by simply growing multiple layers. Furthermore, we have shown that using multiple layers of DMAI-grown alumina for the gate and crossover dielectric results in a large improvement in yield over using a single layer of equivalent thickness grown at the same process conditions.[19] The improvement in yield is a result of the creation of internal interfaces which disrupt the propagation of defects through the thickness of the film.

This process is well suited for building devices of nearly any architecture, and it provides the ability to optimize adjacent devices for different attributes. Devices of different classes could be formed on a single substrate; for example, electronic devices and optical devices could be formed together by choosing materials with the appropriate electrical and optical properties. Depending on the situation, the process can be optimized to minimize the number of process steps, minimize the number of SALD deposition steps, control the interfaces between layers, simplify the layout, simplify the alignment, or any combination of these factors.

TRANSISTOR DESIGN FREEDOM

In any TFT geometry, whether it be bottom or top gate, with staggered contacts or not, there must be a gate conductor layer, a dielectric layer, a semiconductor layer and a source/drain

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electrode conductor layer, with the order of the layers varying for different architectures.[21] (See Figure S2 in the Supporting Information for cross-sectional views of the four different TFT architectures.) Each of these layers can be deposited in a single step, or divided into multiple layers having the same pattern. We have found that there is an improvement in yield that comes with splitting the dielectric layer, independent of device architecture.[19] For bottom-gate TFTs, there is an improvement in the semiconductor−dielectric interface, and therefore TFT performance, when a buffer layer of alumina is formed prior to depositing the semiconductor, using a common inhibitor pattern.[19] These and other modifications to the basic architectures are simple to implement, and can be used with any desired gate dielectric thickness.

Although the patterning and deposition processes impose no constraints on the layer order, the materials and device properties are still influenced by the architecture. We have investigated, for example, bottom-gate ZnO TFTs with staggered and coplanar contacts (Supporting Information Figure S2a,b)). Each device was fabricated (using the inhibitor patterns shown in Supporting Information Figure S3) with 100 nm AZO gate and source/drain, 20 nm ZnO:N semiconductor, and a total of 45 nm Al_2O_3 dielectric divided into 3 layers of 15 nm each. In the staggered structure, the last 15 nm of dielectric was patterned using the semiconductor inhibitor pattern and deposited immediately prior to depositing the ZnO:N. In the nonstaggered geometry, all of the dielectric layers were patterned in the same manner using the dielectric via pattern, and the ZnO was separately patterned and deposited last. The yield was equivalent for both geometries (93% and 94% yield, respectively, for the staggered and coplanar TFTs, with a sample size of 112) and the two structures have equivalent gate leakage. However, the coplanar architecture has a poor subthreshold slope, higher threshold voltage, and lower mobility than the staggered structure with the buffer layer, as can be seen from Figure 2 a). The staggered architecture demonstrates the best-performing enhancement mode devices, with on−off ratios of greater than 10^5 and mobility greater than 10 $cm^2/(V\ s)$.

Using SAD, it is equally simple to fabricate top-gate structures. Both staggered and coplanar top-gate structures were fabricated with 50 nm alumina dielectric, and using the same patterns as for the bottom-gate structures (see Supporting Information Figure S2c,d). As shown in Figure 2b, when top-gate devices are fabricated on glass, they tend to operate in depletion mode, which is to say that their turn-on voltage is less than zero. The two geometries have similar saturation drain current when swept in either the linear or saturation regimes. There was also no difference in yield between the top-gate architectures. The four device architectures illustrated were fabricated simply by changing the order of additive patterned-deposition of the layers

BOTTOM-GATE TFTS AND CIRCUITS

Experimentally, we use inkjet printing to pattern our polymer inhibitor. When using such a digital print technology for device fabrication, the minimum feature size of the printed inhibitor is limited to that of a single printed pixel. For example, the channel in our transistors, defined by our current inkjet-printed inhibitor pattern for the source and drain, is approximately 70−90 μm, depending upon the drop spread for the printing conditions chosen. This minimum achievable feature size has implications on the performance of individual transistors, as

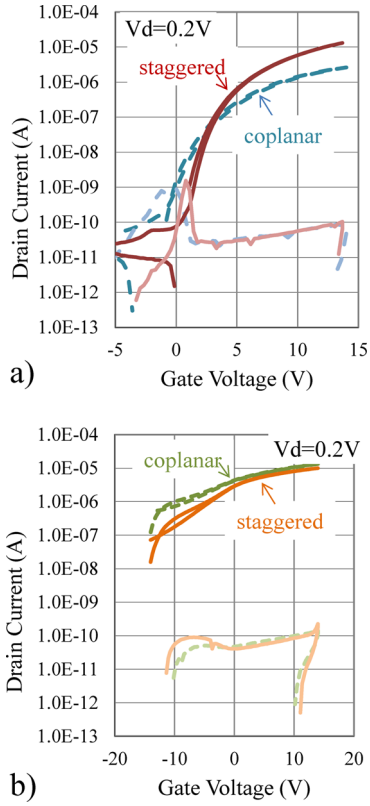

Figure 2. Comparison between staggered and coplanar (a) bottom-gate and (b) top-gate TFTs. For bottom-gate architectures, a staggered structure is preferred and yields enhancement devices. Top-gate transistors operate in depletion mode, with only small differences in performance with contact placement. (Drain current (I_d) and gate leakage current (I_g) are shown for coplanar devices in dashed lines, staggered devices in solid lines; blue = coplanar bottom gate, red = staggered bottom gate, green = coplanar top gate, orange = staggered top gate).

well as the footprint for inverters and circuits. It should be noted, however, that the scale is imposed by our choice of printer and is not inherent to the combination of SAD and SALD.

Typically, when designing all enhancement-mode NMOS inverters (EE), the β-ratio (i.e., the ratio of the aspect ratio W/L of the drive transistor to that of the load transistor, W_{drive}/L_{drive} / W_{load}/L_{load}), is taken as a controlling factor. This aspect ratio, or β-ratio, can be used to predict inverter performance. The assumption inherent in this approach is that the β-ratio gives the ratio of the saturation currents of the two transistors. This follows because in typical circuit design, the field effect mobility and the capacitance of the gate dielectric are equivalent for the drive and load transistors. For β-ratios greater than unity, the gain increases with increasing β-ratio, whereas the minimum output voltage and transition voltage decrease with increasing β-ratio.[22] The switching speed of the inverter is proportional to the average saturation current of the load and drive transistors; therefore, lower β-ratio (near unity) inverters will have faster switching speeds (shorter time-per-stage) for equivalent drive transistor dimensions.[22]

We have fabricated enhancement-mode inverters like the standard circuit illustrated schematically in Figure 3a. Both the drive and load TFTs are staggered bottom-gate transistors, fabricated with a buffer layer to maximize the field effect mobility and a split dielectric to maximize the yield of the large-

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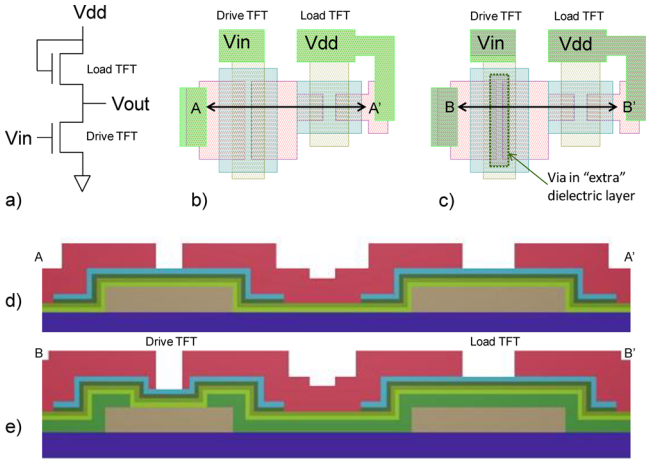

Figure 3. Enhancement-mode inverter illustrations. (a) Schematic equivalent circuit. (b) Example layout of patterned-by-printing inverter with uniform gate dielectric thickness. (c) Example layout of inverter with an extra dielectric layer selectively absent from channel region of drive TFT. (d) Cross-sectional view of drive and load TFTs with uniform gate dielectric thickness. (e) Cross-sectional view of drive TFT with three layers forming gate dielectric, but four layers forming dielectric for load TFT. (Colors in cross sections correspond to those in the plan views: brown = 1st conductor, light blue = semiconductor, red = 2nd conductor, green = dielectric (shown as vias in the plan view)).

area circuits.[19] The drive transistor is sized to provide a large saturation current, with L_{drive} at the minimum of one pixel and W_{drive} chosen to be large, typically a minimum of six pixels. To keep the load, or pull-up, transistor from being too strong, the channel length is increased to be between two and four pixels, while the width is kept small. The semiconductor pattern extends beyond the channel region defined by the separation between the source and drain, which increases the channel width by a predictable fraction through fringing fields.[5] A device layout for an example inverter with a two-pixel design rule is shown in Figure 3b.

Using this base design, without optimization for parasitic capacitance, five-stage ring oscillator circuits were fabricated with an as-designed pixel β-ratio of 2.67. The frequency response of these oscillators was 2.68 kHz at a supply voltage of 20 V.[19] Ring oscillator circuits with other β-ratios show the expected performance variations. By varying the number of stages and the β-ratio of the component inverters, we have fabricated ring oscillators that operate over a range of a few hertz to a few kilohertz, all with a minimum channel dimension of approximately 90 μm.

Although changing the aspect ratio of load and drive TFTs is straightforward, when patterning with a printed technology, the increments are not continuously variable, but must come in pixel units, reducing the flexibility for a circuit designer. However, unlike traditional processing methods, with SAD, it is trivial to independently vary the thickness of the dielectric in adjacent devices. This is accomplished by building up the dielectric thickness using layers having different patterns (see Figure 1). A thinner gate dielectric will result in a larger saturation current, if all other factors are constant. Conversely, because the threshold voltage is proportional to the thickness of the dielectric, increasing the dielectric thickness will decrease current and increase the threshold voltage. This situation gives us an alternative method for sizing the load and drive transistors. We can vary the dielectric thickness of the drive and load transistors independently to optimize an "effective" β-ratio. This approach can be used in combination with the channel dimensions to control the circuit performance and circuit footprint. By decreasing the thickness of the dielectric in the drive transistor, the current can be increased for a smaller footprint. Similarly, the load transistor can be sized by simply increasing the dielectric thickness, or by combining a thicker dielectric with a shorter L for a reduced footprint, in order to achieve a given effective β-ratio. It should be noted that because more than one circuit parameter varies when gate dielectric is

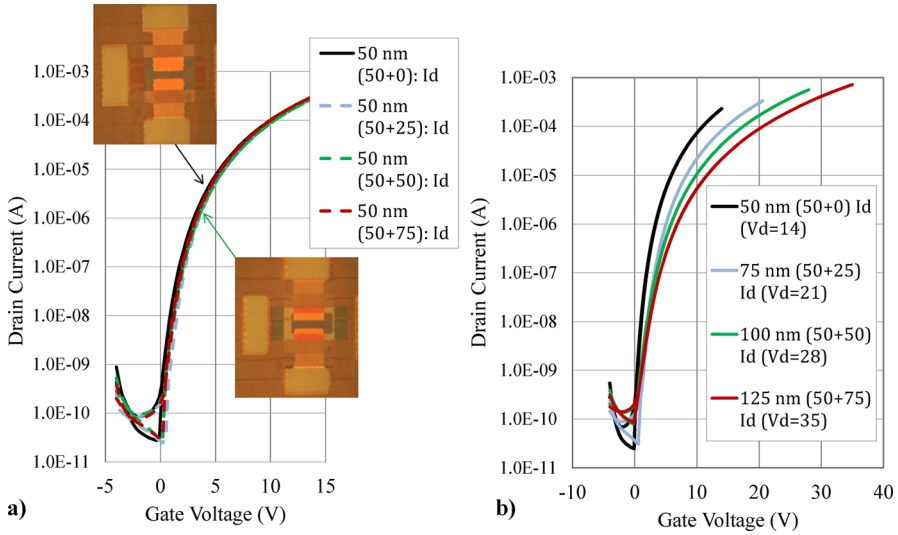

Figure 4. Saturation region performance of bottom-gate TFTs with and without extra dielectric. (a) TFT performance (V_d = 14 V) for TFTs with typical drive TFT design W = 6 pixel/L = 1 pixel. (b) TFTs with design similar to load TFTs with W = 4 pixels/L = 1 pixel and varying amounts of gate dielectric. TFTs with the same gate dielectric thickness in the channel have the same transfer characteristics, with or without the presence of the "extra dielectric". The insets in panel a are micrographs showing the difference in TFT design; the via over the gate for the TFT with the extra dielectric is visible in the lower micrograph. TFTs with design similar to load TFTs of an EE inverter and varying amounts of gate dielectric show the expected increase in threshold voltage and decrease drain current (for a given V_g) as a function of increasing dielectric thickness.

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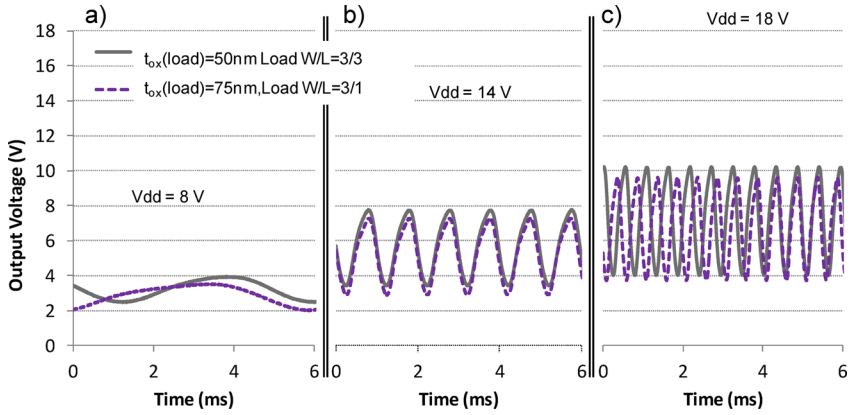

Figure 5. Enhancement mode ring oscillators fabricated with and without 25 nm of extra dielectric, modeled to match at input voltage of 14 V. (a) The output waveform of the ring oscillator at V_{dd} = 8 V; (b) 14 V; (c) 18 V. The design of the circuit with the extra dielectric trades the decrease in current obtained by increasing the dielectric thickness of the load TFT with a reduction in L_{load} to have matched performance at 14 V; as seen in panel b, the shape and frequency are very similar as predicted for the two circuits. Variations in the threshold voltage caused by dielectric thickness differences lead to the extra dielectric circuit having a slower response for V_{dd} less than 14 V, and a faster response at higher voltage, than the uniform dielectric circuit.

varied between drive and load TFTs, circuits will have a different frequency dependence on input voltage than that expected for simple aspect ratio scaling.

To vary the dielectric thickness of the each transistor independently, a new pattern level is needed in addition to the gate, semiconductor, dielectric vias, and source/drain patterns. This new "extra dielectric" pattern can be used to add dielectric to the load TFT without adding additional gate dielectric to the drive TFT. However, by bringing the extra dielectric pattern onto the gate of the drive TFT and opening a via to leave the thinner dielectric only in the center, some additional protection against shorting is provided at the edges of the gate and in the overall device area at crossover points. In addition to the protection against shorting, the extra dielectric reduces the overall capacitance of the drive TFT, the inverter, and ultimately circuits made using these patterns. We size the via in the channel region of the drive transistor to be one pixel larger in all directions than that of the channel. This oversizing allows for variation in alignment, and ensures that the source and drain electrodes make contact to the semiconductor over the portion of the semiconductor having the channel thickness of gate dielectric (minimum amount), to ensure good charge injection.

Figure 3c shows an inverter layout for this alternative approach. The TFT footprints are the same as in Figure 3b, with the difference lying solely in the channel region of the drive TFT where one of the three dielectric layers is "missing". This is seen more easily by comparing schematic cross-sectional views of the inverters through the channels of the drive and load transistors. Figure 3d shows a uniform dielectric thickness, built up by three layers, over both the drive and load gates, whereas Figure 3e shows the first dielectric layer with a gap over the center of the drive TFT gate region.

The transfer curves for individual TFTs (designed to be similar to the drive TFTs in circuits W = 6 pixels and L = 1 pixel) fabricated with and without an extra dielectric pattern, are shown in Figure 4a. All devices had 100 nm AZO gate and source/drain, 20 nm ZnO:N semiconductor, and an aluminum oxide gate dielectric thickness of 50 nm (divided into three layers of 15, 15, and 20 nm). The extra dielectric layer was either omitted (0 nm), as shown in the upper inset of Figure 4a, or patterned to provide 25, 50, or 75 nm of dielectric outside the channel region, as shown in the lower inset of Figure 4a. The extra dielectric layer was deposited between the gate layer and the first layer of the gate dielectric. As expected, electrical performance of the devices formed with this extra dielectric layer is equivalent to performance of those without the extra dielectric layer, because the gate dielectric was not affected. On average, devices formed with the extra dielectric have lower gate leakage, and the leakage decreases as the thickness of the extra dielectric is increased.

The load transistor of the enhancement-mode inverter shown in Figure 3c,e, conversely, is patterned so that the extra dielectric is deposited over the gate in the channel region, allowing the tuning of the dielectric thickness independent of the drive TFT. TFTs patterned like load transistors were fabricated on the same substrates as those in Figure 4a, with a gate dielectric thickness equal to the combined thickness of the gate dielectric of the drive transistor and the extra dielectric. Figure 4b shows the performance of transistors with increasing total dielectric thickness from 50 to 125 nm, and a designed channel of W = 4 pixels and L = 1 pixel. The highest accessible gate voltage scales with dielectric thickness, as does the positive threshold voltage shift, and at any given voltage, there is a significant, and expected, decrease in the saturation drain current. In addition, the gate leakage scales with dielectric thickness.

The predicted current values as a function of drain voltage (V_d), as well as the estimated change in the capacitance of the inverter, can be used to model trade-offs between geometry and dielectric thickness. Using such a model, we designed five-stage extra-dielectric ring oscillators, which would give an equivalent time per stage, at a given input voltage, to those with single common dielectric thickness. For the sake of layout ease and speed, the footprint of the ring oscillators with variable dielectric was chosen to be the same as that of the uniform dielectric oscillators. When optimized, however, the variable dielectric circuit would have a smaller footprint. As designed, the inverters had the same drive TFT channel geometry of W_{drive} = 6 pixels/L_{drive} = 1 pixel and 50 nm gate dielectric. The sample with variable dielectric had 25 nm of extra dielectric outside of the channel region of the drive TFT. The variable dielectric inverter had a load TFT with 75 nm gate dielectric and channel dimensions of W_{load} = 3 pixels/L_{load} = 1 pixel,

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which is predicted to have matched performance, at 14 V, to the circuit with a load TFT with 50 nm dielectric and W_{load} = 3 pixels/L_{load} = 3 pixels. These circuits were evaluated over a range of input voltages, and as can be seen in Figure 5; the performance of these oscillators matches only at a single input voltage. Variation in performance as a function of input voltage is a direct consequence of the dielectric thickness (t_{ox}) impact on both threshold voltage and the relative effect of the gate voltage (field strength). At voltages below the match point, the circuit with smaller load TFTs with a thicker dielectric is slower (longer time per stage); Figure 5a illustrates the longer period of the circuit having the thicker t_{ox} (load). Figure 5b shows that the oscillators exhibit a frequency-matched response of 1 kHz at 14 V, as well as similar swings in output voltage (~4.4 V peak-to-peak). Conversely, the circuit having a thicker dielectric and shorter gate length is faster at higher input voltages than the longer channel length/thinner dielectric circuit; this is illustrated by the response at 18 V, as shown in Figure 5c. The slight offset in output voltage is due to the higher threshold voltage of the thicker-dielectric load TFT ($V_{out\text{-}max} = V_{dd} - V_{th}$).

TOP-GATE TFTS

So far, we have only discussed the use of bottom-gate structures in circuit design. As described above, top-gate TFTs are equally simple to fabricate, and operate as depletion mode devices. We can use this difference in performance from bottom-gate devices to build enhancement-depletion (ED) mode circuits with superior performance to our bottom-gate all-enhancement-mode devices.

Figure 6a,b illustrates the ED equivalent inverter circuit and basic design, using the combination of bottom gate device for drive TFT, and top gate device for load TFT. A schematic cross section of the inverter design with uniform dielectric layer is shown in Figure 6d. The cross section is taken through the channels of the load and drive TFTs, as shown in Figure 6b. To achieve the best enhancement-mode performance from the bottom-gate device, a buffer layer is deposited before the semiconductor.[19] Inverters with top- and bottom-gate TFTs are fabricated by depositing these patterned layers in order (L = load, D = drive, B = both): the first semiconductor (L); first conductor for the gate of the drive TFT and the source/drain of the load TFT (B); the first dielectric (B); second dielectric (B); the second semiconductor pattern with the buffer dielectric and semiconductor material (D); the second conductor to form the source/drain of the drive TFT and the top gate of the load TFT (B).

A portion of the dielectric for the bottom-gate TFT is allocated to the buffer layer, and thus is deposited using the same pattern as the (D) semiconductor. Without compensation, this results in a top-gate load TFT that has less dielectric than the bottom-gate drive TFT in the circuit, as shown in Figure 6d, which can make the load TFT undesirably strong. However, as with the bottom-gate enhancement-mode (EE) circuits, an extra dielectric layer can be used to provide an additional layer of dielectric in the load TFT. This extra dielectric can be used to avoid having to make a larger footprint load TFT (longer channel length) to decrease its strength. That is, it allows one the freedom to independently adjust the dielectric thicknesses to size the relative strength of the drive and load transistors while still using a common dielectric layer.

Substrates with individual top-gate transistors, bottom-gate transistors, inverters, and five-stage ring oscillators were fabricated. All transistors had 100 nm AZO gate and source/drain and 20 nm ZnO:N semiconductor. All bottom-gate transistors had 50 nm total gate dielectric thickness from two dielectric layer patterns (common dielectric) and a buffer layer. Two substrates were fabricated without the use of the extra dielectric pattern, but where the amount of gate dielectric in the top-gate transistor was varied by changing the thickness of the common dielectric. Thus, top-gate TFTs with either 30 or 40 nm dielectric were formed on substrates with bottom-gate devices having 50 nm total dielectric. In the third variation, a 50 nm-thick extra dielectric layer was used in combination with 30 nm of common dielectric to form top-gate TFTs having 80 nm dielectric and bottom-gate devices having 50 nm dielectric.

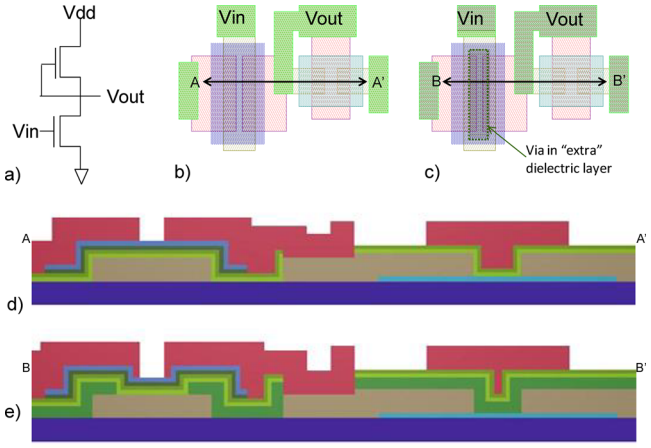

Figure 6. Enhancement-depletion inverter equivalent circuit and layout, with and without an extra dielectric layer, designed from a bottom-gate drive transistor and top-gate load transistor. (a) Circuit schematic. (b) Standard layout with single dielectric pattern (green) and a buffer dielectric below the driver semiconductor (deep green), which is missing from the dielectric stack on the load TFT. (c) Design with an additional dielectric layer with a via in the channel region of the drive transistor. (d) Cross section of ED-mode inverter shown in panel b with a bottom-gate drive TFT and a top-gate load TFT. (e) The extra dielectric layer shown in panel c has a via over the gate of the drive TFT, so that the gate dielectric thickness of the drive TFT is the same in panels a and b. (Colors in cross sections correspond to those in the plan views: brown = 1st conductor, light blue = 1st semiconductor for the top-gate load TFT, dark blue = 2nd semiconductor for the bottom-gate drive TFT, red = 2nd conductor, green = dielectric (shown as vias in the plan view).)

Figure 7 illustrates the current of the top-gate TFT W = 1 pixel/L = 3 pixels, as compared to a typical bottom-gate device with 50 nm total gate dielectric and channel dimensions of W = 12 pixels/L = 1 pixel. When the top-gate TFT has a thin dielectric, the current is higher than that for the bottom-gate TFT for an equivalent field, despite the shorter channel length. In contrast, when the top-gate TFT is fabricated with a thicker dielectric by using an extra dielectric layer, the curves cross at a lower gate voltage/field strength. In these devices, the extra dielectric layer was deposited after depositing the first conductor and prior to depositing the first shared dielectric layer.

These individual top-gate transistors were integrated into inverters with overall geometry shown in Figure 6, and into five-stage ring oscillators. The dimensions (in pixels) of the TFTs in the inverters are W_{drive} = 12/L_{drive} = 1; W_{load} = 1/L_{load} = 3, corresponding to the individual TFT transfer data shown in Figure 7. Figure 8a,b illustrates the expected problem associated with a load TFT that is too strong relative to the

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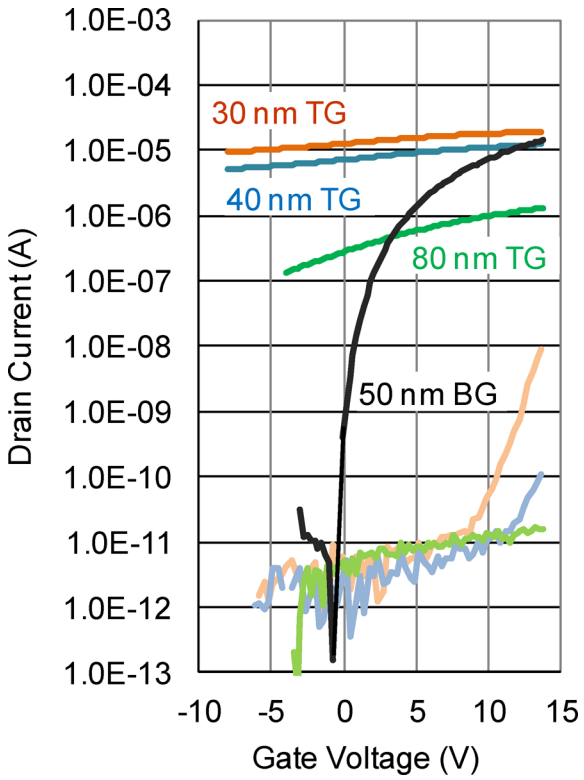

Figure 7. Comparison of linear region transfer curve of top-gate TFTs with 30, 40, and 80 nm-thick dielectric (W = 1 pixel/L = 3 pixels) to a bottom-gate TFT with 50 A dielectric (W = 12 pixels/L = 1 pixel). Devices were tested at Vd = 0.2 V. The top-gate devices with thin dielectric layers have an output current higher than a typical drive TFT, as well as increased gate leakage.

drive TFT of the inverter. Over a reasonable range of input voltages, the inverters without the extra dielectric layer, i.e. inverters whose load TFT has less dielectric (30 nm and 40 nm) than the drive TFT (50 nm), are unable to pull down to ground. The gain of these individual inverters is similarly decreased because of the larger input voltage required for inversion. The inverter having a load TFT with thicker dielectric (80 nm) than the drive TFT (50 nm), however, has a gain of more than 8 as shown in Figure 8b.

The relative frequency response of the five-stage ring oscillators is shown in Figure 8c driven with 18 V. The ring oscillators also had a buffer inverter with characteristic dimensions (in pixels) of $W_{\text{drive-buffer}}$ = 12/$L_{\text{drive-buffer}}$ = 1 and $W_{\text{load-buffer}}$ = 4/$L_{\text{load-buffer}}$ = 3. Although circuits with load TFTs having a thinner dielectric have a poor swing fraction, the frequency response of these devices is higher than that of the thicker dielectric devices. The extra dielectric tunes the oscillator performance to allow the output voltage to swing nearly rail-to-rail, with a corresponding reduction in frequency that is due to the higher equivalent β-ratio and lower average current. This performance is what one from the individual inverter curves in Figure 8a, inverters with a 50 nm extra dielectric layer have a load TFT that can pull the drive TFT down to ground, while the inverters without this extra dielectric have stronger load transistors (thinner dielectric) that are unable to fully pull down the drive TFT over a range of voltages that can be tolerated given their thin dielectric. In fact, the oscillators with thin dielectric have limited operating voltage regimes, because they break down soon after reaching input voltages that are sufficiently high to cause ringing.

For the devices shown in Figure 8, geometry of the devices was kept invariant. However, inverters with load TFTs with different channel dimensions were also fabricated on these substrates. Inverters and ring oscillators with a stronger load TFT (W_{load} = 3/L_{load} = 3) and a dielectric thickness of 80 nm (50 nm extra dielectric layer) exhibits the expected 50% increase in frequency response (reduced time per stage) compared to circuits with the same dielectric and a load TFT of W_{load} = 3/L_{load} = 1, which is due to the increased current of the load transistor. The speed and swing of the circuits can be adjusted by modifying the channel dimensions, the dielectric thickness, or both, for either the drive or the load transistor, providing flexibility in circuit optimization.

In this paper, we have discussed ring oscillators with six different configurations: enhancement-mode oscillators with and without extra dielectric (EE1, EE2), three enhancement-depletion-mode oscillators (ED) with the same geometry and different load TFT dielectric (ED2, ED3, ED4), and one ED-mode oscillator with a load TFT having a modified geometry and a thicker dielectric (ED1). All devices were tested over a range of 8 to 20 V. Figure 9 illustrates the differences in frequency response for two ED circuits and one EE circuit. A summary of the response of all of the oscillator circuits as a function of input voltage, illustrating the expected trade-offs in performance based on the circuit type as well as the relative strength of the load and drive TFTs can be found in Figure S4 of the Supporting Information. The enhancement-mode oscillators (EE1 and EE2) respond over the full voltage range, with a strong frequency dependence on the input voltage, and an output swing less than 40% of the input voltage. As discussed, ED-mode circuits with strong load TFTs are unable to invert the signal at lower V_{dd} voltages, and must be operated at higher voltages. All of the ED-mode oscillators, however, have a greater output voltage swing than the all-enhancement circuits (EE) at all V_{dd} values sufficient for oscillation. Similarly, the frequency response of ED-mode circuits is stable as a function of input (V_{dd}) voltage. While these oscillators were fabricated on different substrates, the selective area process used to fabricate them would readily allow them all to be fabricated on a single substrate. Given the fundamental performance of the ZnO transistors made by this method, peak-to-peak swing and frequency can be predictably controlled using a combination of device architecture, relative channel size, and individual TFT dielectric thickness. This ability to freely mix top-gate and bottom-gate TFTs, as well as enhancement and depletion mode circuitry, is a direct consequence of the additive nature of selective area patterning.

CONCLUSIONS

We have leveraged our previous studies on SAD and SALD to demonstrate how the additive and orthogonal nature of the process brings new design freedoms to thin-film devices. Patterned-by-printing allows the $x-y$ pattern dimensions to be designated and controlled independently from the layer order, individual layer thicknesses, or the material composition of the layers. We demonstrate these freedoms in the area of thin-film electronics, exploiting previously reported process improvements including process robustness from patterns designed for printing alignment and overlap tolerance, increased yield from dividing the dielectric into multiple layers, and improved mobility from controlling the interface between the semi-

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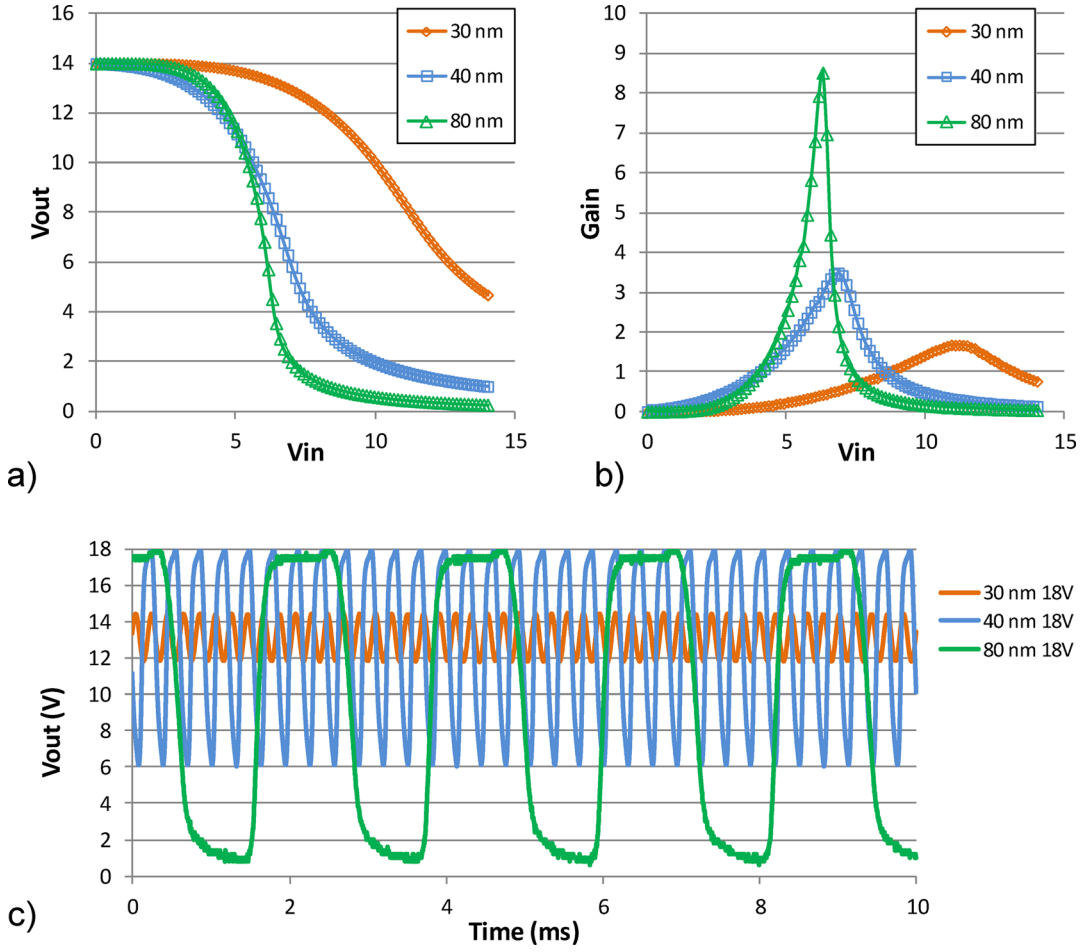

Figure 8. Comparison of inverters with a 50 nm-thick gate dielectric bottom-gate drive TFT and 30, 40, or 80 nm-thick gate dielectric top gate load TFTs, and corresponding five-stage ring oscillator performance. (a) Inverter performance. (b) Inverter gain. (c) Ring oscillator response at V_{dd} = 18 V. The transistor dimensions in pixels are $W_{drive} = 12/L_{drive} = 1$; $W_{load} = 1/L_{load} = 3$. The inverter with the load TFT having a gate dielectric thickness of 80 nm was formed using a 50 nm extra dielectric layer. The inversion voltage decreases with increasing dielectric thickness of the load TFT, while the inverter gain increases with increasing dielectric thickness. The comparison of the output response for five-stage ring oscillators built of the inverters shown in panels a and b illustrate that when properly balanced, enhancement-depletion mode ring oscillators swing rail-to-rail.

conductor and the gate dielectric.[5,19] We have presented a new design element to allow circuits formed from different architectures and having different current requirements. The ability to independently size individual transistors using not just the x-y dimensions of the channel, but also the thickness of the dielectric, has been shown to be an effective and predictable way to further optimize circuits for performance, yield, and footprint. We have demonstrated the use of variable dielectric thickness in both all-enhancement and enhancement-depletion mode circuits. We have further demonstrated the ease of building devices of different architectures with a simple set of three processing tools and a set of basic patterns, by selecting the order in which the layers are deposited in a patterned manner.

We have demonstrated the advantages of patterning using only SAD in combination with SALD using an inkjet printer, which in our lab results in a minimum feature size of approximately 70 μm. There are no fundamental resolution requirements that we are aware of for this technique, and the advantages seen here could be realized by using other inhibitor patterning systems, including higher-resolution print, such as flexography, or by implementing photolithographically defined inhibitor patterns.

We have also shown the relative trade-offs between all-enhancement mode circuits and enhancement-depletion mode circuits made with a mix of bottom- and top-gate devices. All-enhancement circuits are far more sensitive to voltage, which could be used to advantage in some situations, as they have far less voltage swing. Conversely, enhancement-depletion circuits have the ability to swing nearly "rail-to-rail" and can be designed to operate at high frequencies with low sensitivity to voltage.

EXPERIMENTAL SECTION

All experiments were executed using our in-house experimental SALD system, a Fuji Dimatix 2800 inkjet printer, and a Technics PE-IIA plasma system. The experimental atmospheric pressure SALD system operates using a gas-bearing principle and contains two ALD cycles as has been previously described in detail.[7] Square Corning Eagle2000 glass substrates were used (2.5 × 2.5 in. square, 62.5 mm square), and attached using vacuum to a heated backer. The substrate was placed on the purge gas flowing from the SALD coating head, so that it floats above the SALD coating head, and the close proximity of the head and substrate was maintained by the flow of the gases out of and into the head.[7] For all coatings, the exhaust slot pressure was approximately 2.94 Torr. The purge gas and dilution gas was nitrogen. The metal alkyl precursors used for the data in this paper were dimethylaluminum isopropoxide (DMAI) (STREM, 98+%) and diethyl zinc (DEZ)

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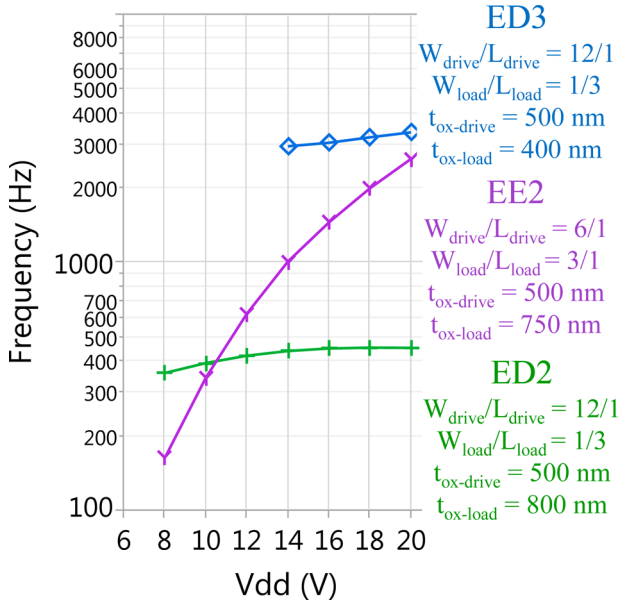

Figure 9. Frequency and time per stage vs voltage for three of the six ring oscillators discussed. All circuits were formed using patterned-by-printing using the same basic process blocks, and have load TFTs with a different gate dielectric thickness than the drive TFT. The relative performance of the all-enhancement (EE) and enhancement-depletion (ED) circuits is as expected, with the ED circuits exhibiting a voltage independent frequency response, while the EE circuit has a strong dependence on V_{dd}.

(STREM, 99.9998%), and the oxygen precursor was water. We use these precursors to grow ZnO (DEZ), Al_2O_3 (DMAI), and AZO, which is formed by flowing a mixture of DEZ and DMAI. Individual mass flow meters controlled the flow rate of the precursor vapor by bubbling nitrogen through the liquid precursor. A flow of ammonia was introduced with the water vapor in order to counter-dope the zinc oxide with nitrogen (ZnO:N). These saturated streams were mixed with a dilution flow before being supplied to the coating device. All bubblers were at room temperature. The partial pressure values can be found in Supporting Information Table S1. The temperature of the coating was established by controlled heating of both the SALD head and the substrate backer.

To fabricate full devices, the glass substrates were cleaned using a 100 W, 0.3 Torr oxygen plasma prior to deposition of the inhibitor. Each inhibitor pattern was printed using the Dimatix printer with a 10 pL cartridge and a solution of 2 wt % PVP k-30 in diacetone alcohol as the ink. After coating, the sample was loaded onto the SALD system and the deposition of the desired layer was accomplished by oscillating the substrate relative to the coating head for the number of cycles necessary to grow a film of the desired thickness for the given example (a round-trip oscillation has four ALD cycles). The precursor exposure time was held constant at 50 ms by controlling the velocity of the substrate to 50.8 mm/s, and the reaction temperature was held at 200 °C. The SALD system operates such that the exposure times for each of the reactive gases and the inert gas (purge) are equivalent.[9] After depositing the patterned layer with the SALD system, the sample was cleaned in a 2 min oxygen plasma to remove the printed inhibitor, and to prepare the surface for the next layer. Specific layer thicknesses are reported for each device; however, typical devices consist of 100 nm-thick conductive gate, 30 to 100 nm-thick insulator, 20 nm-thick semiconductor, and 100 nm-thick conductive source and drain. The complete sequence of substrate cleaning, printing, and SALD steps can take less than 15 min, which means that complete devices can be fabricated in approximately 1 h. Electrical testing was performed using an automated probe station and an Agilent 4155C parameter analyzer. The ring oscillators were driven using an Agilent 6613C 0−50 V power supply, and the response was recorded using a Tektronics TDS 2024B oscilloscope.

■ ASSOCIATED CONTENT

Supporting Information

Inhibitor patterns, transistor geometry cross sections, and reactant partial pressure data. This material is available free of charge via the Internet at http://pubs.acs.org.

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Author Contributions

The paper was written through contributions of all authors. All authors have given approval to the final version of the paper.

Notes

The authors declare no competing financial interest.

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